

ISSCC 2016 Reports Program (2016/2/17)

Session Chair	Time		Title	Speaker(Affiliation)
	9:30 9:35		Opening	<u>Takeshi Yamamura</u> (Fujitsu Laboratories)
	9:35 10:00		Review of ISSCC 2016	<u>Atsuki Inoue</u> (Fujitsu Laboratories)
Professor Iizuka Univ. of Tokyo	10:00 10:25	4.4	A 197mW 70ms-Latency Full-HD 12-Channel Video-Processing SoC for Car Information Systems	<u>Seiji Mochizuki</u> (Renesas System Design)
	10:25 10:50		A 16nm FinFET Heterogeneous Nona-Core SoC Complying with ISO26262 ASIL-B: Achieving 10 ⁻⁷ Random Hardware Failures per Hour Reliability	<u>Chikafumi Takahashi</u> (Renesas System Design)
	10:50 11:15	4.5	4Mb STT-MRAM-Based Cache with Memory-Access-Aware Power Optimization and Write-Verify-Write / Read-Modify-Write Scheme	<u>Hiroki Noguchi</u> (Toshiba)
	11:15 12:05	7.2	(Invited) 5G Technologies and Development in 2020 and Beyond	<u>Takehiro Nakamura</u> (NTT Docomo)
	12:05 13:30		Lunch	
Professor Ikeda Univ. of Tokyo	13:30 13:45		A 1280×720 Single-Photon-Detecting Image Sensor with 100dB Dynamic Range Using a Sensitivity-Boosting Technique	<u>Mitsuyoshi Mori</u> (Panasonic)
	13:45 14:00	6.6	A 1.2e- Temporal Noise 3D-Stacked CMOS Image Sensor with Comparator-Based Multiple-Sampling PGA	<u>Kei Shiraishi</u> (Toshiba)
	14:00 14:25	6.7	CMOS Biosensor IC Focusing on Dielectric Relaxations of Biological Water with 120GHz and 60GHz Oscillator Arrays	<u>Takeshi Mitsunaka</u> (Sharp)
	14:25 14:50	28.3	A 768Gb 3b/cell 3D-Floating-Gate NAND Flash Memory	<u>Tomoharu Tanaka</u> (Micron)
	14:50 15:15	7.7	A 65nm CMOS ADPLL with 360μW 1.6ps-INL SS-ADC-Based Period- Detection-Free TDC	<u>Akihide Sai</u> <u>Satoshi Kondo</u> (Toshiba)
	15:15 15:40	19.7	A 56Gb/s NRZ-Electrical 247mW/lane Serial-Link Transceiver in 28nm CMOS	<u>Takayuki Shibasaki</u> (Fujitsu Laboratories)
	15:40 16:15	3.5	Break	
Professor Ito Tokyo Institute of Tech.	16:00 16:25		A 56Gb/s W-Band CMOS Wireless Transceiver	<u>Korkut Tokgoz</u> <u>Kenichi Okada</u> (Tokyo Institute of Tech.)
	16:25 16:40	13.3	A 42Gb/s 60GHz CMOS Transceiver for IEEE 802.11ay	<u>Rui Wu</u> <u>Kenichi Okada</u> (Tokyo Institute of Tech.)
	16:40 17:05	13.6	A 300GHz 40nm CMOS Transmitter with 32-QAM	<u>Kosuke Katayama</u> (Hiroshima Univ.)
	17:05 17:30	20.1	17.5Gb/s/ch Capability over 6 Channels	<u>Hidenori Okuni</u> (Toshiba)
	17:30 17:45	26.1	A 5.5mW ADPLL-Based Receiver with Hybrid-Loop Interference Rejection for BLE Application in 65nm CMOS	<u>Ken Yamamoto</u> <u>Yuya Kondo</u> (Sony)
	17:45 17:55	26.5	A 0.7V 1.5-to-2.3mW GNSS Receiver with 2.5-to-3.8dB NF in 28nm FD-SOI	
	17:45 17:55		Closing	<u>Makoto Nagata</u> (Kobe Univ.)

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