Call for Papers

Submission Deadline

The deadline is November 7, 2016

IEEE CICC is sponsored by the IEEE Solid-State Circuits Society and the IEEE Electron Devices Society

Hotel Van Zandt, *Austin Texas*
April 30 – May 3, 2017

The IEEE Custom Integrated Circuits Conference (CICC) is the premier conference devoted to IC development. CICC emphasizes the education of experienced engineers as well as students while showcasing original, first-published innovative analog and digital circuit techniques covering a broad spectrum of technical topics. It is a forum for circuit, IC and SoC designers, CAD developers, manufacturers and ASIC users. CICC is the conference to find out how to solve design problems and improve circuit design and chip design techniques.

Conference Highlights

Technical Sessions addressing a broad range of circuits, applications, design techniques, tools, test, reliability, and emerging technologies, and providing education on new, state-of-the-art developments is the core of the CICC technical program.

Educational sessions instructed by recognized invited speakers who are among the best in the industry are included in the conference. They are valuable opportunities to refresh key skills in traditional circuit-design methods and acquire knowledge in vital new areas in analog, digital, and RF integrated circuit design

Panels, ***Forums*** and a ***Plenary Session*** provide a platform for leaders from the IC industry and academia present highlights on new field of research and development related to circuit design and to debate key issues and controversial topics. CICC panels are well known for their lively and thought-provoking discussion and audience participation.

Our ***Exhibits*** are where semiconductor manufacturers, IP providers, SW tool suppliers, design-service houses, and technical book publishers offer of their products.

Our ***Welcome Reception***, ***Conference Reception***, ***Conference Luncheon*** bring additional opportunities for discussion and peer networking.

CICC is soliciting papers in the following areas:

Power Management circuits and techniques for power generation, conversion, distribution, monitoring and integration aimed to reduce overall energy consumption and increase power efficiency including adaptive techniques, IP/SOC/System level power and thermal management techniques, regulators, DC-DC converters, power control and management circuits, energy-harvesting and wireless power circuits.

Analog Circuits and Techniques for areas such as communications, biomedical, aerospace, automotive, energy, environment, computing and security applications, ranging from basic building blocks to silicon sensors, interfaces, and novel clock generation architectures.

Data Converters of all types enabled by new techniques, architectures, or circuit topologies.

Wireless Transceivers and RF Circuits for low-power and energy-efficient links, biomedical and wireless sensor networks and IoT applications, cellular connectivity including M2M applications (LTE-M, NB-IoT), emerging broadband and MIMO networks (5G, WLAN), millimeter-wave and THz systems (radar, sensing and imaging).

Wireline Communications Circuits and Systems for electrical and optical communications, including serial links and components for intra-chip and chip-to-chip interconnections, high-speed memory and graphics interfaces, backplanes, long-haul, and power line communications.

Design Foundations: modeling, simulation, manufacturing, and testing, to improve design quality and design efficiency. Topics include modeling of advanced CMOS (e.g., FinFET, FD-SOI) and beyond-CMOS devices (e.g., GaN, Non-Volatile

Memories) design methodologies for emerging applications (deep learning, automobile, IoT, security), and design for manufacture, test, and reliability (novel DFT circuits, system-level testing, SoC verification).

Emerging Technologies solicits hardware focused papers in the technologies of tomorrow. This includes, but is not limited to, biomedical SOCs, sensors and MEMS, hardware based machine learning, emerging memories, silicon photonics, disruptive digital design, large area electronics, implementations in non-CMOS and hybrid process technologies.

Submission of Papers

Paper Submission deadline is November 7, 2016

Papers must report original and previously unpublished work, including specific results. Papers may be up to 4 pages in length including illustrations, charts, tables and references. Successful submissions concisely explain how the work advances the state of the art and include schematics, measured results, and technical detail sufficient to be understood. **Circuit-design papers intended for traditional lecture presentation must include measured experimental results that substantiate performance claims.** Circuit-design papers using only simulation to substantiate performance claims are usually rejected for traditional lecture presentation, but may be considered for poster presentation.

Papers are submitted electronically. **Prior** to preparing your paper for electronic submission, please read the paper preparation and submission guidelines on the CICC website (www.ieee-cicc.org). The submission instructions are available and the submission page will be active early September 2016. Go to the CICC website at www.ieee-cicc.org and click on Papers and Presentations.

When submitting a paper, please indicate a preference for traditional lecture or poster presentation, although CICC may assign presentations to either category.

Deadline for submission of technical papers is November 7, 2016. Appropriate company and government clearances MUST be obtained prior to submission. AUTHORS MUST SUBMIT a completed copyright form at the time of paper submission. If a copyright form is not received with the submission, the paper will not be reviewed. Authors of accepted papers will be notified by email by January 15, 2017.

ACCEPTED PAPERS WILL BE PRINTED IN THE PROCEEDINGS WITHOUT OPPORTUNITY FOR FURTHER CHANGE.

Accepted papers will be used for publicity purposes and portions of these papers may be quoted in pre-conference magazine articles and also via the Web. If this is not acceptable, authors must email CICC at cicc@his.com to decline publicity.

Awards include **Best Paper** and **Best Student Paper**. Top-rated papers are also eligible for publication in a special issue of the **IEEE Journal of Solid State Circuits** and the **IEEE Transactions on Circuits Systems**.

For Further Information

For complete author kit instructions, registration information, and general inquiries visit the CICC website at www.ieee-cicc.org or contact the Conference Office: IEEE Custom Integrated Circuits Conference, 19803 Laurel Valley Place, Montgomery Village, MD 20886, Telephone: 301/527-0900 x1, Fax: 301/527-0994, email: melissaw@widerkehr.com, web page: http://www.ieee-cicc.org.

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Visit the CICC web site for complete instructions on submitting a paper.
Web address: www.ieee-cicc.org
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