

Advanced Program

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Conference Time Table

Time: Eastern European Summer Time (UTC+3)

Wednesday	Thursday	Friday
October 11th	October 12th	October 13th
	11:20-12:20	11:50-12:50
	Regular Session 2	Regular Session 3
		12:50-13:00
		Closing Ceremony
13:00-14:00	13:00-14:00	13:00-14:00
Lunch	Lunch	Lunch
14:00-14:30	14:00-18:00	
Opening Ceremony	Trip to "Cantacuzino"	
	Castle, Busteni	
14:40-15:40		
Invited Talk		
16:10-17:10		
Regular Session 1		
		20:30-
		Banquet including
		Best paper award ceremony

^{*} AVIC 2023 is held concurrently with CAS 2023. Please see the "CAS 2023 program overview".

Opening Celemony Speech

Speaker Prof. Pat Cunneen, Analog Devices, Romania



Biography Pat Cunneen joined Analog Devices in June 1976 as HR Manager as part of a small start-up team. While his Analog career spanned 26 years, his first 12 years was directly involved in the leadership of the Irish business including recruitment, people development and organisational culture. Subsequent AD roles included HR manager at the then largest AD site in Wilmington Massachusetts and later was appointed Director of HR for the newly created Worldwide Manufacturing Organisation. He has a B.Comm from UCD, an MBS from UL, was a Fellow of CIPD (UK), an Adjunct Professor of Strategic HR at the University of Limerick and has published 3 books.

Invited Talk

Wednesday October 11th 14:40–15:40

Chairman: Prof.

Speaker Prof. Arcadie Cracan, Gheorghe Asachi Technical University of Iaşi, Romania

Title Resistance to digital, resistive sensing, highly digital SAR ADC, delta-sigma DAC, and bitstream DAC

Abstract This work presents a highly digital successive approximation direct resistance to digital converter. To achieve a high level of digital domain circuitry, an oversampling delta-sigma digital to analog converter is used. The remaining analog domain circuitry consists of an integrator used as an error amplifier for which the output voltage is proportional to the difference between the measured and the approximated resistance and a comparator to detect the sign of the approximation error. To further reject high-frequency quantization noise, an up/down counter is utilized at the output of the comparator. The implemented resistance to digital converter achieves a 7-bits resolution and a 5-bits accuracy (as validated by simulation).



Biography Prof. Cracan has received his BSc in electronics engineering (2008) and his PhD in electronics and telecommunications engineering (2011) from Gheorghe Asachi Technical University of Iasi (TUIASI), Romania. In 2011 he joined the Fundamentals of Electronics department of TUIASI where he is assisting and lecturing courses in analog and digital circuits design and testing. His research interests include analog sensors, analog signal processing, analog-to-digital and digital-to-analog conversion, radio-frequency circuits design, digital signal/image processing, power conversion systems. He is currently the Head of the Fundamentals of Electronics department at TUIASI and is a consultant for Infineon Romania in Iaşi. Dr. Cracan has authored or coauthored over 30 international journal and conference proceedings papers. He is a member of the IEEE Solid-State Circuits Society and IEEE Education Society and serves as a reviewer for several MDPI journals.

Wednesday October 11th 14:40–15:40

Chairman: Prof.

Speaker Prof. Marius Neag, Technical University of Cluj-Napoca, Romania

Title Analog and hybrid fast-transient-eesponse LDOs able to handle a wide ranges of load currents and capacitors

Abstract This invited talk is as the following contents:

- Brief presentation of the "Digitally Enhanced RF and Analog IC" Research Group at the Technical University of Cliij-Napoca
- Examples of University-Industry cooperation: the PartEnerIC and iDev4.0 projects
- Methodologies for systematic design of PMICs based on multi-physics simulators
- PMICs for automotive applications: SC DC-DC converter with High BW Power Mirror and Dual Supply Driver & Slew-Rate Booster and Frequency Compensation Circuit for Automotive LDOs
- Novel approaches to the analysis and design of a class of Any-Cload Fast LDOs



Biography Prof. Neag graduated the M.Eng. program on Applied Electronics at the Technical University of Cluj-Napoca (TUCN), Romania, in 1991 and was awarded the Ph D. degree by the University of Limerick, Ireland, in 1999. After several years working as a senior designer of RF, analog and mixed-signal ICs in Ireland, the UK and the US he returned to the academia. Since 2008 he is an Associate Professor with the TUCN, where he co-founded the "Digitally Enhanced RF and Analog IC" Research Group. He has co-authored over 30 articles published in prestigious journak papers and more than 100 papers presented at international scientific conferences, as well as 4 books on Analog IC design, as well as 3 international patents. Assoc. Prof. Neag has been an active IEEE member since 1994, with substantial contributions to several Societies and the IEEE Romania Section. He is currently the Vice-chair of both the Education Society and the Solid-State Circuits Society, Romania Section, and serves as Counselor of the IEEE Student Branch at the Technical University of Cluj-Napoca, a Student Branch he helped established in 2020. Since 2018 he is a member of the Committee for Microsystems Science and Technology of the Romanian Academy.

Regular Session

Wednesday October 11th 11:10–12:30

Session 1: RFs and Analog Circuit 1

Chairman: TBA

(R-1) A zero temperature coefficient voltage reference: stability and versatility using 28nm FD-SOI technology

Maxime Guillot*, Yann Deval, Hervé Lapuyade (Université de Bordeaux, France); Kawori Sekine, Kazuyuki Wada (Meiji University, Japan); François Rivet (Université de Bordeaux, France)

(R-2) A walsh-based arbitrary waveform generator for 5G applications in 28nm FD-SOI CMOS technology

Pierre Ferrer*, François Rivet, Hervé Lapuyade, Yann Deval (Université de Bordeaux, France)

(R-3) Verification of element selection methods for multi-coil electric motor driving Yoshiaki Ishikawa*, Akira Yasuda (Hosei University, Japan)

Thursday October 12th 16:40–17:40

Session 2: Analog Circuit 2

Chairman: TBA

- (R-4) A method for OPamp sizing using model-based reinforcement learning Kazuya Yamamoto*, Nobukazu Takai (Kyoto Institute of Technology, Japan)
- (R-5) The improvement of SNDR by passive signal-residue summation with the switched capacitor integrator of the noise-shaping successive approximation register ADC

 Sho Saito*, Akira Hyogo, Tatsuji Matsuura, Ryoichi Miyauchi (Tokyo University of Science, Japan)
- (R-6) Proposal and application of equivalent MOSFET with different temperature coefficient of threshold voltage

Hiroshi Kobayashi*, Kawori Sekine, Kazuyuki Wada (Meiji University); François Rivet, Hervé Lapuyade, Yann Deval (Université de Bordeaux, France)

Friday October 13th 10:40-12:00

Session 3: Analog Circuit 3

Chairman: TBA

- (R-7) A Multi-bit $\Delta\Sigma$ down-converting ADC with even-harmonic mixer and mismatch shaper Takumi Shibata*, Kiichi Yamashita, Yuki Genkaku, Yasuhiro Sugimoto, Akira Yasuda (Hosei University, Japan)
- (R-8) Development of a sensor buoy equipped with a chlorophyll-a concentration measurement system using image spectrum analysis

Shunya Kosako*, Toshihiko Hamasaki (Hiroshima Institute of Technology, Japan)

(R-9) Analysis of the distortion characteristics of guitar amplifiers caused by different tube amplification factors

Karin Sakamoto*, Toshihiko Hamasaki (Hiroshima Institute of Technology, Japan)

Note: * is a presenter.